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IPLEMENTATION OF MULTLILEVEL INVERTER BASED DYNAMIC VOLTAGE RESTORER

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Abstract: Dynamic voltage restorer (DVR) is a power electronic converter-based custom power device used to compensate for voltage variations. The inverter used in the DVR structure can have different topologies. Multilevel inverters are a good candidate to be used in the DVR structure especially in higher voltage level. This study proposes a new scheme for DVR based on a multilevel inverter. In the proposed DVR, a dc–dc converter is attached to the multilevel inverter. The dc-link voltage is regulated by the dc–dc converter considering the voltage sag magnitude. In this way, the output voltage of the multilevel inverter has always its maximum possible number of levels. This results in better quality of output voltage in both deep and shallow voltage sags. It is important to emphasise that the existing inverter-based DVR topologies do not have this capability. Also, in the proposed DVR, there is no need for an output filter. Moreover, the fundamental frequency control method for the multilevel inverter can be used instead of pulse width modulation-based methods. This can result in lower switching losses and lower switching stresses. The mathematical analysis of the operation range of the proposed DVR is given in detail. The simulation results using Power System Computer Aided Design/Electromagnetic Transient including DC (PSCAD/EMTDC) as well as the experimental results from a laboratory prototype verify the proposed DVR scheme.

1 Introduction

Sensitive loads such as computers, electronic devices and automated systems are vulnerable to voltage variations. Voltage variations include various events. The voltage variations are divided into two events, short-term and long-term events. The short-term events may be compensated for by suitable devices. These events mainly include the voltage sags, voltage swells and short-term interruptions. In many distribution power systems, the voltage sags are the most frequent and economically the most damaging event [1]. Therefore investigating suitable ways to compensate for the voltage sags is an important issue.

Many solutions are available for the compensation of voltage disturbances [2–4]. The power electronic-based solutions are the most suitable solutions because of flexibility and fast response. According to the literature, Dynamic voltage restorer (DVR) is the most suitable and economical solution to compensate for voltage sags. In fact, the DVR is a series connected voltage source inverter (VSI). It generates compensation voltage which is added to the grid voltage usually through an injection transformer. In this way, the voltage on the sensitive load remains almost unchanged providing for safe operation of the loads [5].

Many variant DVR circuit topologies are available. The VSI as the main part of the DVR can have different circuit topologies. The conventional two-level or multilevel VSIs can be adopted in the DVR. When discussing the control methods or dynamic analysis, the simplest form of inverter is usually used in the DVR structure. However, as an alternative, using multilevel inverters in the DVR structure has been addressed in some published matters. A cascaded *H*-bridge (CHB) multilevel inverter-based voltage sag compensator has been presented in [6] which is controlled by using the fundamental frequency control method. Therefore as the output voltage is a stepped voltage, the output voltage quality is not acceptable for some operating points. The pulse width modulation (PWM) controlled CHB multilevel inverter application to the DVR has been investigated in [7]. In this work, both symmetric and asymmetric topologies have been considered. The CHB multilevel inverters need an isolated dc voltage source per each *H*-bridge. Reference [8] investigates the application of the transformer coupled CHB multilevel inverter for the DVR in which only one dc voltage source is required. From the control method point of view, minimum power operation of the DVR based on the CHB multilevel inverter has been studied in [9]. A modified DVR based on the CHB multilevel inverter has been presented in [10]. In this topology, in order to reduce the size of energy storage, the DVR is equipped with a thyristor controlled reactor. In [11], discontinuous space vector modulation (SVM) to control the CHB multilevel inverter used in the DVR has been presented. Apart from the CHB topologies, other multilevel inverters such as the neutral point clamped (NPC) multilevel inverter [12–13], and the flying capacitor multilevel inverter [14] have also been used in the DVR structure. Moreover, other non-conventional topologies of

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multilevel inverters have been used in the DVR structure [15, 16].

The VSIs are the dominant power electronic converters used in the DVR structure. However, recently various circuit configurations have been presented for the DVRs which use ac–ac converters instead of VSIs [1, 5, 17–19]. Therefore the energy storage elements are eliminated in these topologies resulting in possible reduction in the overall size of the DVR. However, as they are not equipped with energy storage elements, their operation in the case of deep voltage sags may not be successful. Also, a three-phase nine-switch converter-based compensator has been presented in [20]. Moreover, the application of the DVR to provide a fault ridethrough of the distributed energy resources has been addressed in [21].

Considering the literature review presented above, different types of multilevel inverters have been in the DVR structure to generate the required compensating voltage. However, the main issue considering the multilevel inverter-based DVR is the fact that the output voltage of the multilevel inverter varies depending on the voltage sag depth. Clearly, for deep voltage sags the output voltage magnitude should be high and inversely for shallow voltage sags it is low. This implies that if the dc-link voltage is considered to be constant then the number of output voltage levels depends on the voltage sag depth. For shallow voltage sags, the number of voltage levels must be reduced. In other words, the multilevel inverter will not generate the output voltage with maximum possible number of levels unless for a narrow band of deep voltage sags. Consequently, the multilevel inverter will not be exploited suitably in the case of lower voltage sags. Therefore it seems that the application of the multilevel inverters in the DVR structure is not very successful especially for shallow voltage sags.

In this paper, a new scheme is proposed for multilevel inverter-based DVR for better utilisation of the multilevel inverter. The dc–dc converter is used to adjust the dc-link voltage considering the depth of voltage sag. Using this method, the maximum possible number of output voltage levels is generated for a wide variation of voltage sag depths. In this way, the quality of the output voltage is improved by reducing the filtering requirements. In Section 2, the proposed DVR is presented and then its operation range is calculated. In order to verify the proposed DVR, the simulation and experimental results are presented.

2 Proposed DVR

The proposed multilevel inverter-based DVR is shown in Fig. 1*a*. In the proposed topology the dc-link voltage is adjusted by considering the voltage sag depth. The energy storage has a constant dc output voltage (V_{in}). This voltage is the input voltage of the dc–dc converter. The task of the dc–dc converter is to adjust the dc-link voltage (V_{dc}) according to the voltage sag depth. In other words, for voltage sags that have a lower depth, the value of V_{dc} is reduced and inversely as the voltage sag depth is high, the value of V_{dc} is increased. In this way, the multilevel inverter reference voltage is always high and therefore it operates with a high modulation index regardless of the voltage sag depth. Therefore all the possible output voltage levels are generated within a wide range of voltage sags [22].

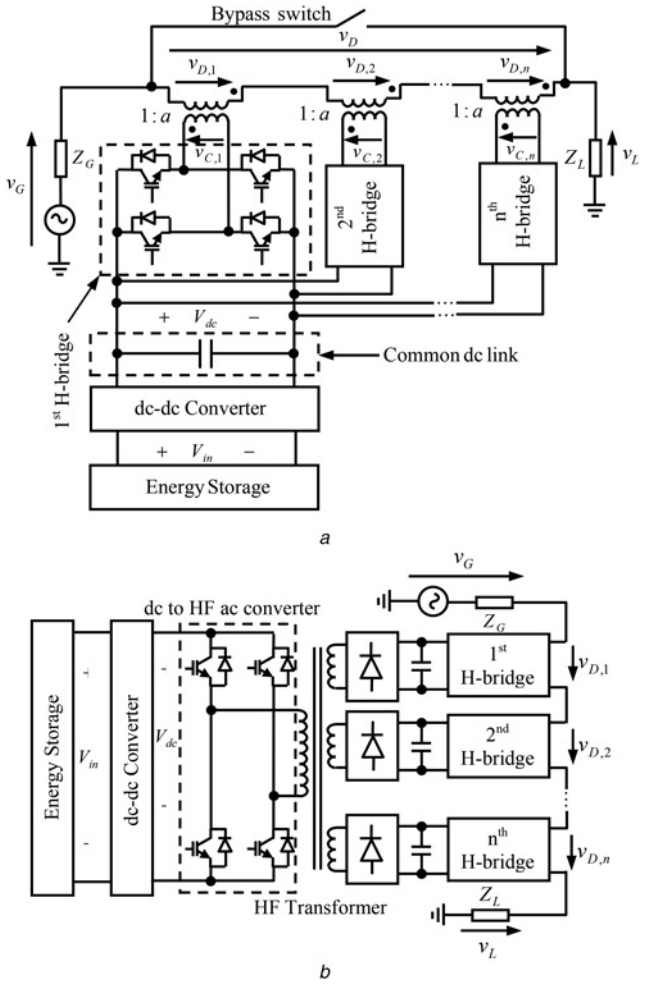

Fig. 1 *Proposed DVR*

In the DVR presented in Fig. 1*a*, one low-frequency transformer is needed per each *H*-bridge. This may cause

a The proposed multilevel inverter-based DVR
b Proposed alternative topology for the DVR

the system to be costly. However, the transformer can boost the voltage so that the inverters operate in lower voltage even if the operational voltage is high. As an alternative topology, high-frequency (HF) transformers can be used instead of low-frequency transformers. This alternative topology is shown in Fig. 1*b*. In this topology, the dc output voltage of the energy storage is fed to a dc–dc converter. The dc–dc converter adjusts its output voltage according to the value of voltage sag (similar to the previous topology). The output dc voltage of the dc–dc converter is then converted to an HF ac voltage. The HF ac voltage supplies the primary side of an HF transformer with multiple secondary. In the secondary, the HF ac voltage is converted to a dc voltage feeding the *H*-bridges of the multilevel inverter. The HF transformers provide isolation so that the output of the *H*-bridges can be connected in series. The basic idea of this topology is similar to the previous one. Therefore the rest of the paper relies on the topology shown in Fig. 1*a*.

In a multilevel inverter, the quality of the voltage is directly related to the number of voltage levels and it improves as the number of voltage levels increases. Consider the staircase output voltage of a cascaded multilevel inverter as shown in Fig. 2*a*. The *h*th harmonic of the output voltage can be written as follows

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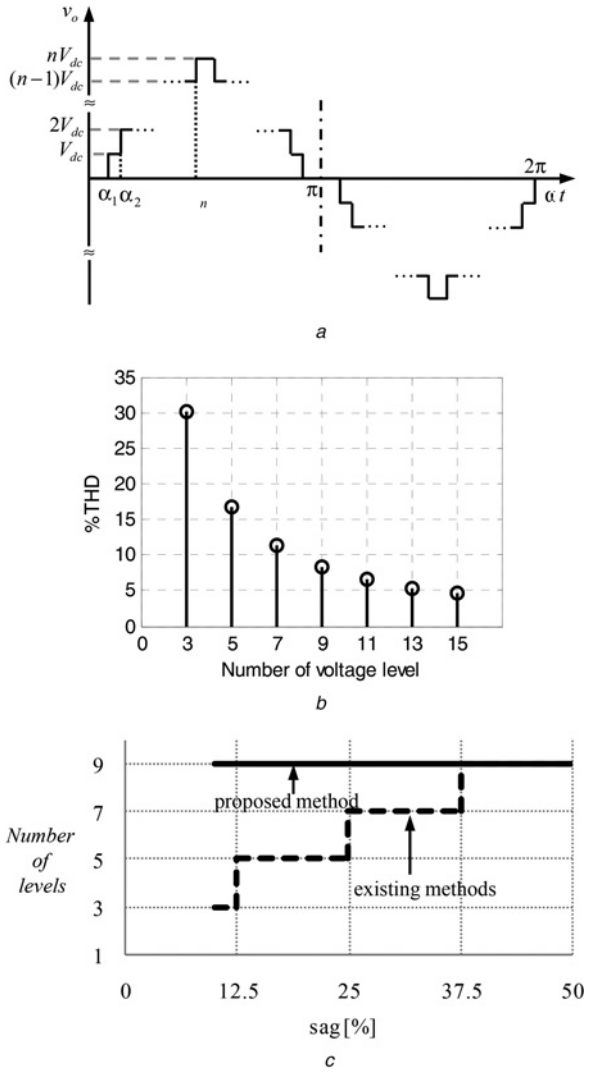

Fig. 2 *Typical operation of cascaded multilevel inverter*
a Typical staircase output voltage of a multilevel inverter
b Variation of THD percentage of the staircase voltage against number of voltage levels
c Number of voltage levels of the multilevel inverter output voltage against sag percentage for the proposed and existing methods

$$V_{o,h} = \frac{1}{\pi}\int v_o(t)\sin(h\omega t)\, d(\omega t) = \frac{4V_{dc}}{h\pi}\sum_{i=1}^{n}\cos h\alpha_i \quad h:\text{odd} \tag{1}$$

Total harmonic distortion (THD) of the output voltage can be written as follows

$$\text{THD} = \frac{\sqrt{\sum_{h=3,5,\ldots}^{\infty} V_{o,h}^2}}{V_1} = \frac{\sqrt{\sum_{h=3,5,\ldots}^{\infty} V_{o,h}^2}}{V_1}$$

$$V_{o,1} = \frac{\sqrt{2}}{2\sqrt{2}V_{dc}}\sum_{i=1}^{n}\cos\alpha_i \tag{4}$$

where α_i depends on the control method of the multilevel inverter. For the nearest level control method [23–24], α_i can be stated as follows

$$\alpha_i = \arcsin\frac{i-0.5}{n} \quad i = 1, 2, \ldots, n \tag{5}$$

Using the above calculation, the variations of THD of the output voltage against the number of voltage levels is shown in Fig. 2*b*. This figure shows that as the number of voltage levels increases the THD is reduced. Therefore for an *N*-level inverter it will be more suitable to generate output voltage with *N* levels in all range of operating points. Using a dc–dc converter with variable output voltage to supply the dc-link of the multilevel inverter makes this idea possible. In the proposed DVR, for different voltage sag depths the number of output voltage levels is maximum resulting in a considerably better waveform quality. Although the proposed approach can be applied for any multilevel inverter topology, in this paper, the CHB multilevel inverter is used. Different circuit topologies can be considered for the proposed system. If the multilevel inverter has one common dc-link, only one dc–dc converter is required otherwise for each *H*-bridge an independent dc–dc converter is needed. In order to use one common dc-link, an injection transformer for each *H*-bridge is required. It is worth mentioning that the transformers act as injection transformers at the same time. The *H*-bridges are supplied from one common dc-link and their output voltages are added together via the injection transformers. The total resulting voltage is the injection voltage which compensates for the voltage sag.

Several power quality (PQ) surveys showed that the voltage sags include more than 90% of all PQ problems. Moreover, considering the data gathered from the surveys, most voltage sags are lower than 0.5 pu (0.5 pu remaining voltage) [25, 26]. Suppose that a multilevel inverter-based DVR is designed to compensate for a maximum 0.5 pu voltage sag. Fig. 2*c* shows the number of voltage levels of the multilevel inverter used in the DVR structure for the proposed and existing methods against voltage sag percentage. In this figure, the multilevel used in the DVR structure is a nine-level inverter. Using the conventional multilevel inverter-based DVRs, for the voltage sags up to 0.125 pu the output voltage will be a three-level voltage. From 0.125 up to 0.25 pu it will be a five-level voltage, from 0.25 to 0.375 pu the output voltage is a seven-level voltage and from 0.375 to 0.5 pu the output voltage will be a nine-level voltage. For this example, only for 0.25 of operation range the output voltage will have its maximum

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$$\text{THD} = \frac{\sqrt{V_{o,rms}^2 - V_{o,1}^2}}{V_{o,1}} \quad (2)$$

The total RMS ($V_{o,rms}$) and the RMS value of the fundamental component ($V_{o,1}$) of the output voltage can be obtained as follows

$$V_{o,rms} = \sqrt{\frac{2}{p}\left(2V_{dc}\sum_{i=1}^{h}\frac{\cos(h\alpha_i)}{h}\right)^2} \quad (3)$$

possible number of levels (i.e. nine levels). It is important to note that the proposed DVR can operate with its maximum possible number of voltage levels for almost the whole operating range. Moreover, unlike the conventional multilevel inverter-based DVRs, the multilevel inverter used in the proposed DVR always operates with the modulation index equal to 1 which improves the output voltage quality. Two ways are available to control the output of the inverter: variation of the modulation index and variation of the input dc voltage. In the proposed DVR, the input dc voltage of the multilevel inverter is variable and controllable because of usage of the dc–dc converter. Therefore the output

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voltage is controlled by varying the input dc voltage of the multilevel inverter whereas its modulation index can be constant. In order to generate the maximum possible number of voltage levels, the modulation index should be equal to its maximum value which is 1. These are analysed in detail in the next sections.

High value of THD and harmonic contents results in higher losses, temperature and de-rating of the transformers. As studied in [27] the transformer power rating decreases extremely with the increase of harmonic contents. Therefore reduction of the THD and harmonic contents of the output voltage can result in reduction in the ratings and size of the injection transformers and also has a positive effect on their lifetime.

In the conventional two-level or three-level inverter-based solutions, in order to achieve an output voltage with acceptable quality and also reduce the output filter size, the HF modulation method should be used. This results in higher stresses on the switches, switching losses and higher electromagnetic interferences (EMI). In the proposed DVR it is possible to use the fundamental frequency modulation method without losing the output voltage quality. This modulation method results in reduction in the number of commutations in each period which affects the switching losses, stresses and EMI. As the control of the multilevel inverter in the proposed DVR is based on the fundamental frequency method, the output voltage of the multilevel inverter does not contain HF contents as in the PWM method. Also, the proposed DVR operates in a way that the number of output voltage levels remains high. Therefore the output filter is not required in the proposed topology.

3 Compensating limits

In this section, the compensating limits of the DVR are calculated. Owing to the fact that any part of the DVR such as the input dc voltage, the dc–dc converter, and the transformer has its own limitation, the calculations are presented in a general form. The aim is to calculate a range for the voltage sag in which maximum number of voltage levels is possible. Even though the calculations are simple, they are important to design the DVR.

Applying Kirchhoff's voltage law (KVL) for Fig. 1, the following equation can be obtained

$$v_{\mathrm{L}}(t) = v_{\mathrm{G}}(t) + v_{\mathrm{D}}(t) \tag{6}$$

where v_{L}, v_{G} and v_{D} represent the load voltage, grid voltage and the DVR injected voltage, respectively. It is important to note that v_{D} is sum of the output voltages of the CHBs, in other words

$$v_{\mathrm{D}} = v_{\mathrm{D},1} + v_{\mathrm{D},2} + \cdots + v_{\mathrm{D},n} \tag{7}$$

If the peak values of the voltages are considered, (6) can be rewritten as follows

$$V_{\mathrm{L}} = V_{\mathrm{G}} + V_{\mathrm{D}} \tag{8}$$

Defining V_C as follows

be obtained

$$V_{\mathrm{D}} = aV_C \tag{10}$$

The voltage sag definition is as follows

$$V_{\mathrm{sag}} = V_{\mathrm{L,ref}} - V_{\mathrm{G}} \tag{11}$$

where $V_{\mathrm{L,ref}}$ is the peak value of the load voltage in nominal condition. If the DVR completely compensates for the load voltage, the peak value of the load voltage will be always equal to its nominal value as follows

$$V_{\mathrm{L,ref}} = V_{\mathrm{L}} \tag{12}$$

Considering (8) and (10)-(12), the following equation is achieved

$$V_C = \frac{V_{\mathrm{sag}}}{a} \tag{13}$$

The peak value of the output voltage of the multilevel inverter (V_C) is related to the dc-link voltage (V_{dc}) by the modulation index (M) and the number of CHBs (n), which can be written as follows

$$V_C = nMV_{\mathrm{dc}} \tag{14}$$

The relation between the input voltage of the dc–dc converter (V_{in}) and the dc-link voltage can be expressed as the voltage transfer ratio of the dc–dc converter (k) as follows

$$k = \frac{V_{\mathrm{dc}}}{V_{\mathrm{in}}} \tag{15}$$

Substituting (14) and (15) in (13), the following equation can be written

$$V_{\mathrm{sag}} = anMkV_{\mathrm{in}} \tag{16}$$

Using (16), the following equation can be written

$$k = \frac{V_{\mathrm{sag}}}{anMV_{\mathrm{in}}} \tag{17}$$

It is clear that in a multilevel inverter the number of output voltage levels is maximum if M is close to 1. Hence, k should be variable so that the output voltage of the dc–dc converter could be adjusted. The range of k can be considered as follows

$$k_{\min} \le k \le k_{\max} \tag{18}$$

Considering the limits stated by (18), (16) can be rewritten as follows

$$anMk_{\min}V_{\mathrm{in}} \le V_{\mathrm{sag}} \le anMk_{\max}V_{\mathrm{in}} \tag{19}$$

The range of voltage sag stated by (19) is the range in which

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the voltage sag can be completely compensated for with maximum number of output voltage levels and a given value of *M*.

$$V_C = V_{C,1} + V_{C,2} + \cdots + V_{C,n} \quad (9)$$

Using (9) and considering Fig. 1, the following equation can

It is better to state (19) in per-unit. If the peak value of the load voltage is the base of voltage ($V_L = 1$ pu), then the range

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can be rewritten as follows

$$\frac{anMk_{\min}V_{\text{in}}}{V_{\text{L}}} \le V_{\text{sag}}^{\text{pu}} \le \frac{anMk_{\max}V_{\text{in}}}{V_{\text{L}}} \tag{20}$$

Let M vary within the following range

$$M_{\min} \le M \le M_{\max} \tag{21}$$

Then, the voltage sag range stated by (21) can be rewritten as follows

$$\frac{anM_{\min}k_{\min}V_{\text{in}}}{V_{\text{L}}} \le V_{\text{sag}}^{\text{pu}} \le \frac{anM_{\max}k_{\max}V_{\text{in}}}{V_{\text{L}}} \tag{22}$$

It is important to note that although in (22) M varies within a range. Still, with a limited range maximum possible number of output voltage levels are generated.

To have a better view of the voltage sag range, the variation of per-unit value of voltage sag, which can be compensated for with maximum possible number of voltage levels is shown in Fig. 3 against a and k. The figure shows that a or k, or both increase, the maximum compensable voltage sag increases. However, a is considered to be constant and k plays the role of adjusting the dc-link voltage.

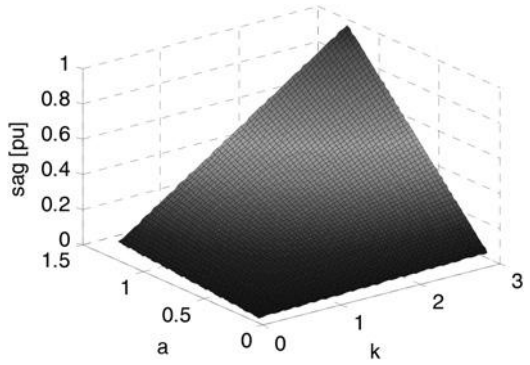

Fig. 3 *Variations of the voltage sag that can be compensated for by maximum possible number of voltage levels against a and k*

Table 1 Voltage transfer ratio limits of the dc–dc converters

dc–dc converter	$k_{\min}$	$k_{\max}$
buck	0	1
boost	1	practical limit
buck-boost	0	practical limit

Table 1 shows the limits of the voltage transfer ratio of the dc–dc converter ($k_{\min}$ and $k_{\max}$). As the table shows, the limits depend on the type of dc–dc converter and practical issues.

4 Simulation and experimental results

The proposed DVR has been simulated in the PSCAD/EMTDC software and its laboratory scale has been implemented. The simulation results as well as the experimental results are presented in order to demonstrate the operation of the proposed DVR. For simulation and experimentation, a nine-level case is selected which is shown in Fig. 4. The reason behind this selection is that according to Fig. 2*b* the THD is inversely related with the number of levels and the effect of the number of levels in the value of THD is considerable as the number of voltage levels varies from 3 to 9. In continuity, as the number of voltage levels increases the decrement of THD is lowered. However, as the number of voltage levels increases, the number of required power electronic switches also increases. Therefore a tradeoff between the value of THD and number of switches should be considered. Considering these factors, the nine-level case is selected in this paper. It is clear that by choosing a higher number of voltage levels the quality of output voltage will improve considerably. In order to adjust the dc-link voltage a boost dc–dc converter is used in this paper. However, other dc–dc converters such as buck converter can be also used. The main parameters of the studied system are indicated in Table 2. In the experimental tests, a fault generator is used to generate voltage sag. The fault generator consists of a three-tap transformer with three bidirectional switches. Depending on the states of the switches three values are available for the grid voltage. If the switch S_1 is turned on,

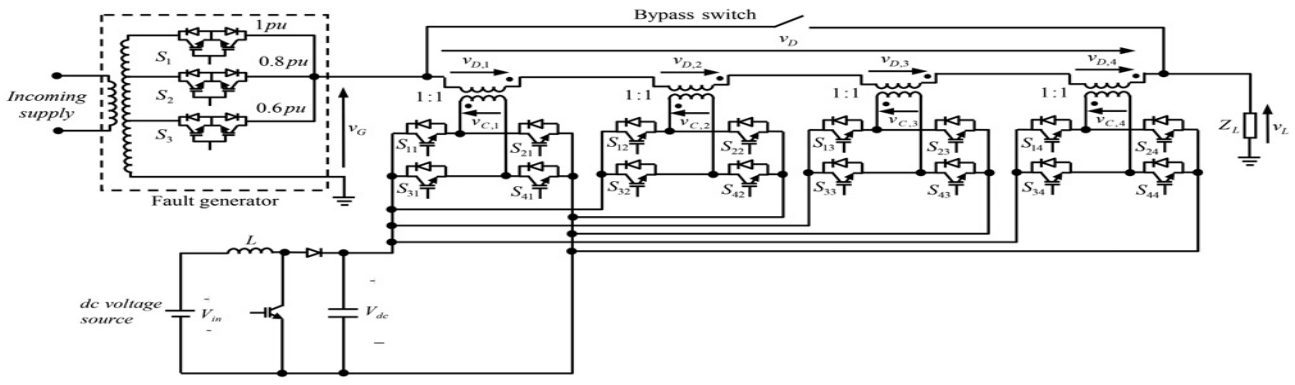

Fig. 4 *Nine-level inverter-based DVR used for simulation and experimentation*

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Table 2 Main data of the studied system

Parameter		value
boost dc–dc converter	L, μH	80
	k_{min}	1
	k_{max}	3
load	R, Ω	45
	L, mH	55
injection transformer	Impedance, Ω	0.45 + j3.5
	Turns ratio (a)	1
dc-link capacitor, μF		5000
frequency, Hz		50
voltage peak in normal condition, V		$220\sqrt{2} = 1$ pu
number of CHBs (n)		4

the grid voltage will be 1 pu which indicates the normal operation condition without any voltage sag. By turning on the switches S_2 and S_3, the grid voltage will be 0.8 pu (0.2 pu sag) and 0.6pu (0.4 pu sag), respectively.

As the number of CHBs (n) and also the turns ratio of the injection transformer are predetermined in Table 2, the only design parameter is the input voltage of the dc–dc converter. It can be determined so that the most severe expected voltage sag is completely compensated for. Using (20), the input voltage of the dc–dc converter (V_{in}) in terms of maximum voltage sag that should be compensated for can be obtained as follows

$$V_{in} = \frac{V_{sag,max}^{pu} V_L}{anMk_{max}} \quad (23)$$

As a numerical example, suppose that the aim is to compensate for voltage sags up to 0.5pu (i.e. $V_{sag,max}^{pu} = 0.5$ pu). Using (23) and the data given in Table 2, the value of the input dc voltage of the dc–dc converter (V_{in}) is obtained as follows

$$V_{in} = \frac{0.5 \times 220\sqrt{2}}{1 \times 4 \times 1 \times 3} \approx 13\,\text{V}$$

With this value of the dc voltage and considering the lower limit given by (20), the lowest value of the voltage sag is $V_{sag,max}^{pu} = 0.16$ pu. Therefore the proposed multilevel inverter-based DVR with the given data, can compensate for voltage sags between 0.16 and 0.5 pu with a nine-level output voltage. This means that it operates with its maximum number of voltage levels within a wide range of voltage sags. It is important to note that this is not possible in the other multilevel inverter-based DVRs.

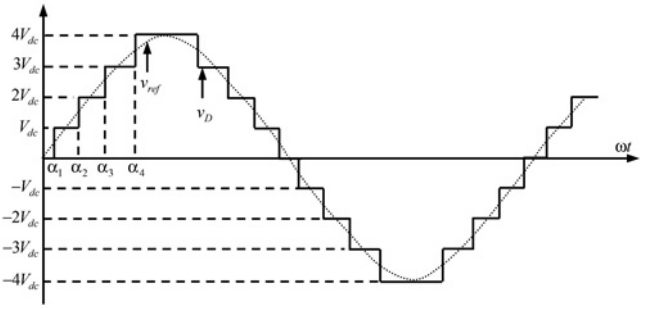

Fig. 6 *Principle operation of the NLC method*

Fig. 5 shows the control diagram of the DVR. The measured voltage of the grid (v_G) is subtracted from the reference voltage ($v_{L,ref}$) to obtain the voltage sag (v_{sag}) which is also equal to the reference value of the DVR output voltage. Using this value, the voltage sag is detected. If the value of this quantity exceeds a certain threshold, the voltage sag is detected and the control system is detected.

In order to regulate the load voltage, a feedback control with PI controller is used in addition to the feed-forward loop. The output of this feedback and feed-forward control is divided by the dc-link voltage and used as the reference for multilevel inverter control. In order to control the multilevel inverter, the nearest level control (NLC) method [28] is used. Fig. 6 shows the principle of this control method for a nine-level inverter [29]. In this method, the reference voltage is compared with the available voltage levels and the nearest level is selected by choosing the corresponding switching combination from the switching table. For example when the reference voltage is in the limits $0.5V_{dc} < v_{ref} < 1.5V_{dc}$, the voltage level equal to V_{dc} is

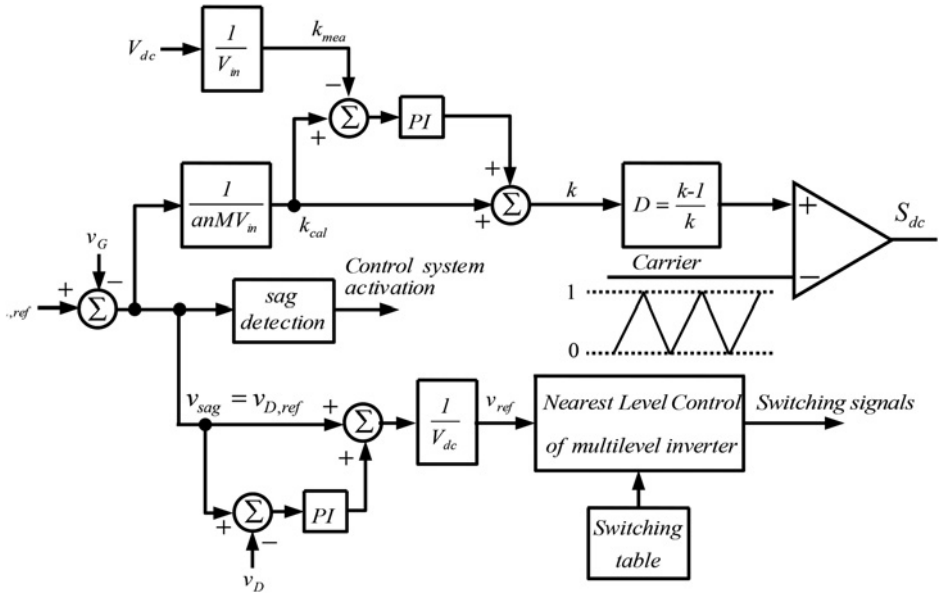

Fig. 5 *Control strategy of the DVR*

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Table 3 Reference voltage limits, selected voltage levels and the corresponding ON switches

Reference voltage limits	Selected voltage level	ON switches
$0 \le v_{ref} < 0.5V_{dc}$	0	S_{11}, S_{31}, S_{12}, S_{32}, S_{13}, S_{33}, S_{14} and S_{34}
$0.5V_{dc} \le v_{ref} < 1.5V_{dc}$	V_{dc}	S_{11}, S_{41}, S_{12}, S_{32}, S_{13}, S_{33}, S_{14} and S_{34}
$1.5V_{dc} \le v_{ref} < 2.5V_{dc}$	$2V_{dc}$	S_{11}, S_{41}, S_{12}, S_{42}, S_{13}, S_{33}, S_{14} and S_{34}
$2.5V_{dc} \le v_{ref} < 3.5V_{dc}$	$3V_{dc}$	S_{11}, S_{41}, S_{12}, S_{42}, S_{13}, S_{33}, S_{14} and S_{34}
$3.5V_{dc} \le v_{ref}$	$4V_{dc}$	S_{11}, S_{41}, S_{12}, S_{42}, S_{13}, S_{43}, S_{14} and S_{44}

selected which is the nearest voltage level and the corresponding switches are turned on. Table 3 shows the reference voltage limits, selected voltage level and the corresponding ON switches in the NLC method. It should be noted that this table is for the positive half-cycle. The table can be simply extended to the negative half-cycle by replacing the ON switches by their complementary counterparts. As Fig. 5 shows, the reference voltage of the multilevel inverter is obtained by dividing the value of voltage sag by the dc-link voltage. For a lower value of the voltage sag the dc-link voltage is also low and therefore the reference voltage of the multilevel inverter remains high. To control the dc–dc converter, its voltage transfer ratio (k) as stated by (15) is considered. This value of k is used in the feed-forward loop. However, for better regulation of the output voltage of the dc–dc converter a feedback loop with a PI controller is also used. In the feedback loop, the measured value of k (obtained by dividing the measured V_{dc} by V_{in}) is subtracted from its value obtained using (17) and the result is applied to a PI controller. The output of the feedback and feedforward loops is used to control the dc–dc converter. As the output of this stage is the voltage transfer ratio of the dc–dc converter, it should be converted to the duty cycle (D) in order to be used for providing the switching signal of the dc–dc converter. Therefore the duty cycle is calculated from the voltage transfer ratio. By comparing the duty cycle with an HF triangular carrier waveform the switching signal of the dc–dc converter is obtained.

4.1 Simulation results

The simulation results of the voltage sag compensation using the proposed topology are shown in Fig. 7*a*. To show that the proposed topology generates the output voltage with maximum number of levels for different voltage sag depths, two different voltage sags with different depths are applied on the grid voltage. The first voltage sag occurs from 0.02 to 0.12 s whose depth is 0.2 pu. The second voltage sag starts at 0.14 s and lasts for 0.1 s with a depth of 0.4 pu. In both the voltage sags, the dc–dc converter adjusts the dc-link voltage considering the voltage sag depth. Therefore the DVR output voltage is a nine-level voltage in both cases. To make this easy to observe, two enlarged views of the DVR output voltage are shown. The THD percentage of the DVR output voltage is 10 and 10.2 for the 0.2 and 0.4 pu voltage sag, respectively. As the output voltage quality remains acceptable in different voltage sags, the filter capacitor has not been used in the structure of the proposed DVR. Fig. 7*b* shows the output voltages of the bridges of

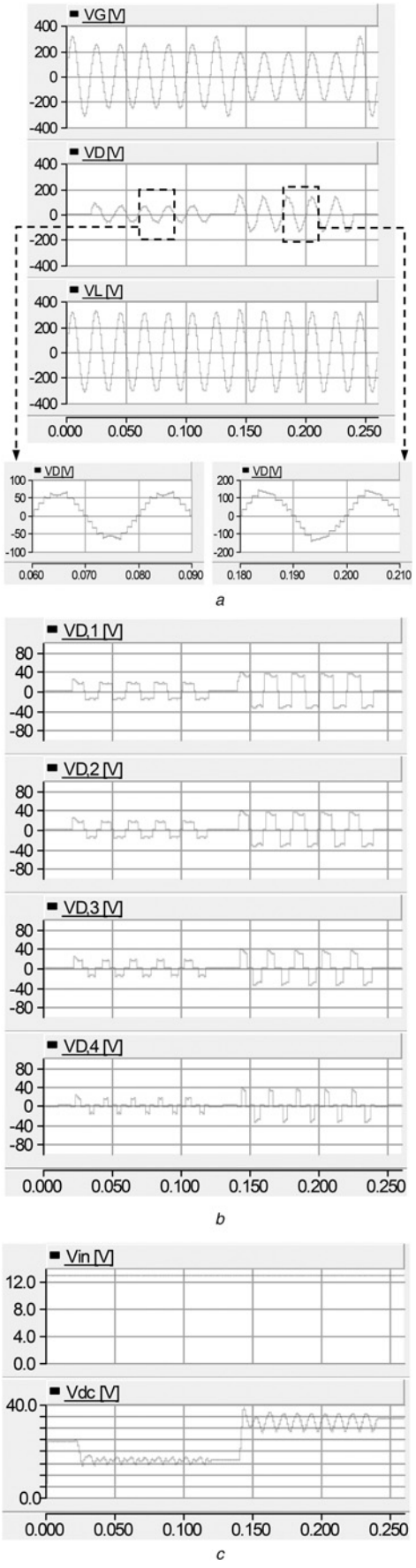

Fig. 7 *Simulation results of the proposed DVR*

a From top to bottom the traces are the grid voltage, injected voltage, the load voltage and enlarged view of the injected voltage in two different conditions
b Top to bottom: $v_{D,1}$, $v_{D,2}$, $v_{D,3}$ and $v_{D,4}$
c Upper: input voltage of the dc–dc converter, lower: dc-link voltage

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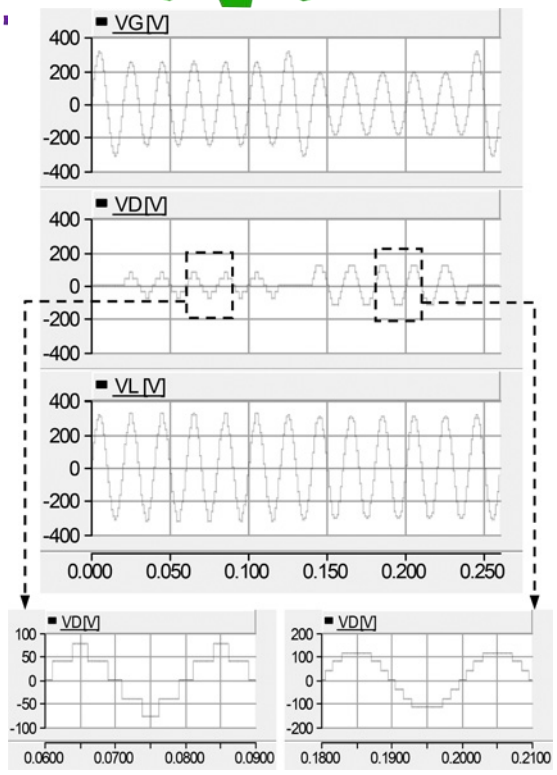

Fig. 8 *Simulation results of a conventional multilevel inverter-based DVR; from top to bottom the traces are the grid voltage, injected voltage, the load voltage and enlarged view of the injected voltage in two different conditions*

the multilevel inverter ($v_{D,1}$, $v_{D,2}$, $v_{D,3}$ and $v_{D,4}$). As the figure shows, the bridges operate in fundamental frequency and each one generates a three-level voltage. The sum of these voltages is equal to the DVR injected voltage. The upper trace in Fig. 7*c* shows the input voltage of the dc–dc converter. As the figure shows, this voltage is a constant voltage equal to 13 V according to the design example. The lower trace in Fig. 7*c* shows the output voltage of the dc–dc converter or

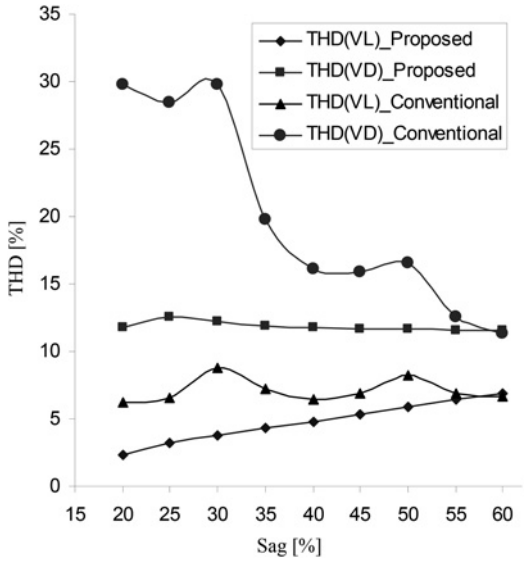

Fig. 9 *THD comparison of the proposed DVR with the conventional CHB-based DVR without adjusting dc voltage employing fundamental frequency control method*

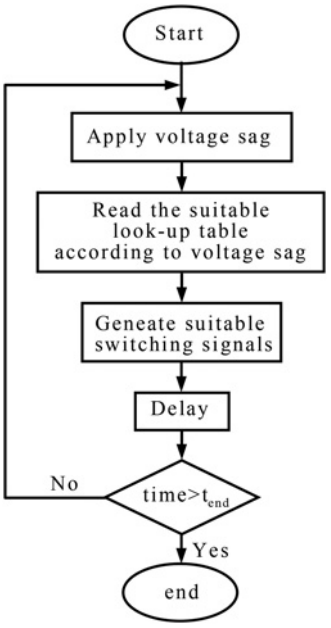

Fig. 10 *Algorithm flowchart implemented in the microcontroller to control the DVR*

the dc-link voltage. As the figure shows, the dc-link voltage is adjusted according to the value of the voltage sag. The fluctuation of the dc-link voltage with the frequency of double of the fundamental frequency is a common event in single-phase systems and it will not be present in the balanced three-phase systems.

Fig. 8 shows the simulation results of the conventional multilevel inverter-based DVR with the same condition. As this figure shows, the number of levels of the DVR output voltage varies as the amount of voltage sag varies. In the case of a 0.2 pu voltage sag the number of voltage levels is five and in the case of a 0.4 pu voltage sag, the number of voltage levels is seven. Therefore in none of the sag conditions the maximum number of voltage levels is generated (the maximum number of levels is nine). It is important to note that the DVR is designed to compensate

Table 4 Switching table and the corresponding switching method

Interval	Voltage level	ON switches
$0 \le \omega t < 7.18°$, $172.82° \le \omega t < 180°$	0	S_{11}, S_{31}, S_{12}, S_{32}, S_{13}, S_{33}, S_{14} and S_{34}
$7.18 \le \omega t < 22°$, $158° \le \omega t < 172.82°$	V_{dc}	S_{11}, S_{41}, S_{12}, S_{32}, S_{13}, S_{33}, S_{14} and S_{34}
$22 \le \omega t < 38.68°$, $141.32° \le \omega t < 158°$	$2V_{dc}$	S_{11}, S_{41}, S_{12}, S_{42}, S_{13}, S_{33}, S_{14} and S_{34}
$38.682 \le \omega t < 61°$, $119° \le \omega t < 141.32$	$3V_{dc}$	S_{11}, S_{41}, S_{12}, S_{42}, S_{13}, S_{43}, S_{14} and S_{34}
$61° \le \omega t < 119°$	$4V_{dc}$	S_{11}, S_{41}, S_{12}, S_{42}, S_{13}, S_{43}, S_{14} and S_{34}
$180 \le \omega t < 187.18°$, $352.82° \le \omega t < 360°$	0	S_{21}, S_{41}, S_{22}, S_{42}, S_{23}, S_{43}, S_{24} and S_{44}
$187.18 \le \omega t < 202°$, $338° \le \omega t < 352.82°$	$-V_{dc}$	S_{21}, S_{31}, S_{22}, S_{42}, S_{23}, S_{43}, S_{24} and S_{44}
$202° \le \omega t < 218.68°$, $321.32° \le \omega t < 338°$	$-2V_{dc}$	S_{21}, S_{31}, S_{22}, S_{32}, S_{23}, S_{43}, S_{24} and S_{44}
$218.682° \le \omega t < 241°$, $299° \le \omega t < 321.32°$	$-3V_{dc}$	S_{21}, S_{31}, S_{22}, S_{32}, S_{23}, S_{33}, S_{24} and S_{44}
$241° \le \omega t < 299°$	$-4V_{dc}$	S_{21}, S_{31}, S_{22}, S_{32}, S_{23}, S_{33}, S_{24} and S_{44}

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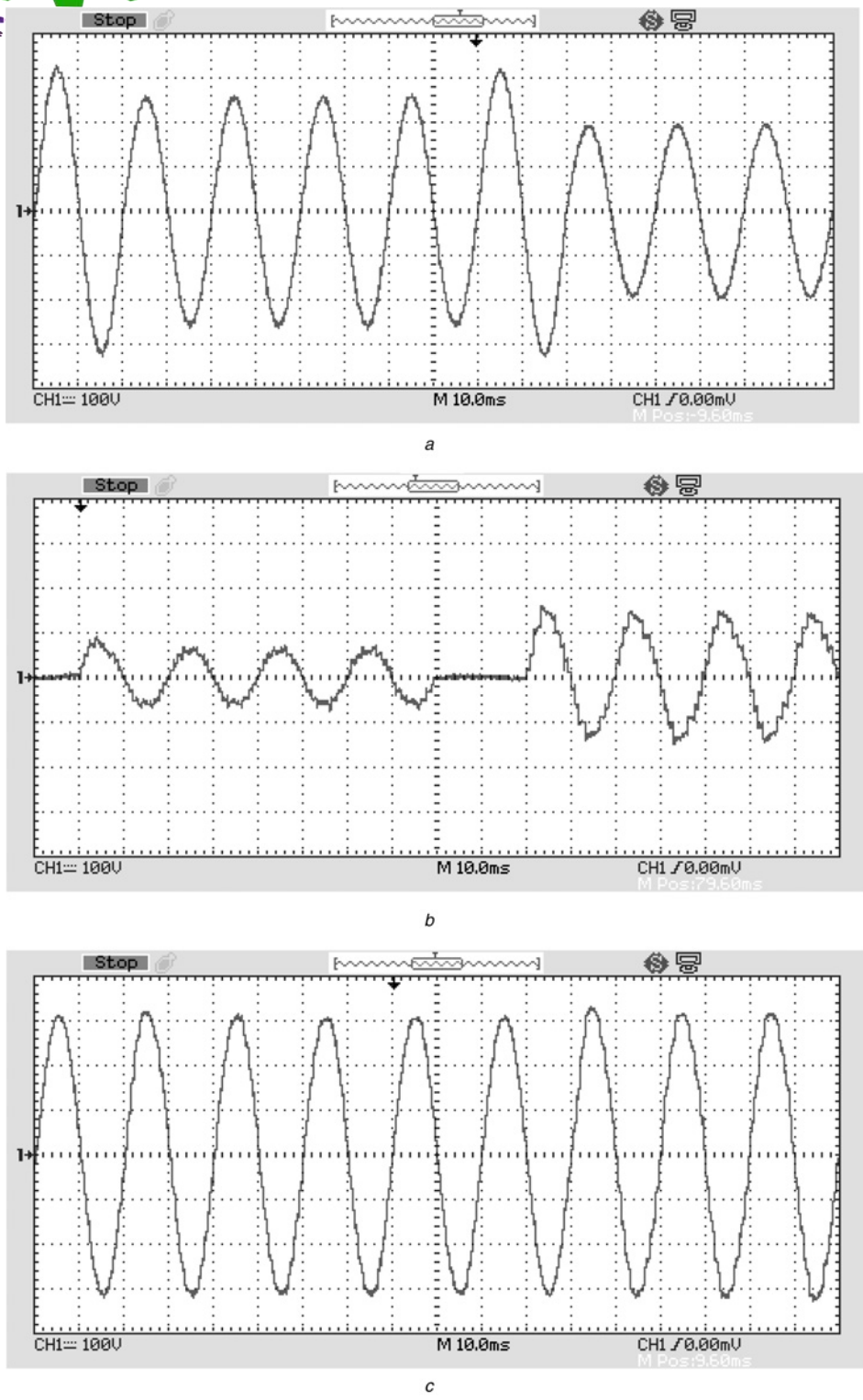

Fig. 11 *Experimental results*

a Grid voltage
b DVR injected voltage
c Compensated load voltage

for maximum 0.5 pu voltage sag and for voltage sags between 0.4 and 0.5 pu the output voltage will be a nine-level voltage. The THD percentage of the output voltage for the conditions of 0.2 and 0.4 pu voltage sag is 28 and 11, respectively, which are higher than that of the proposed approach (especially for lower voltage sag).

A simulation-based comparison on the quality of the load voltage and DVR output voltage has been performed between the proposed DVR and the conventional CHB multilevel inverter-based DVR without dc–dc converter to change the dc-link voltage. The results of this comparison are shown in Fig. 9. This figure indicates the THD percentage against the sag depth for the DVR output voltage and load voltage in both the proposed and conventional DVR. In this comparison, the fundamental frequency control method has been considered for the

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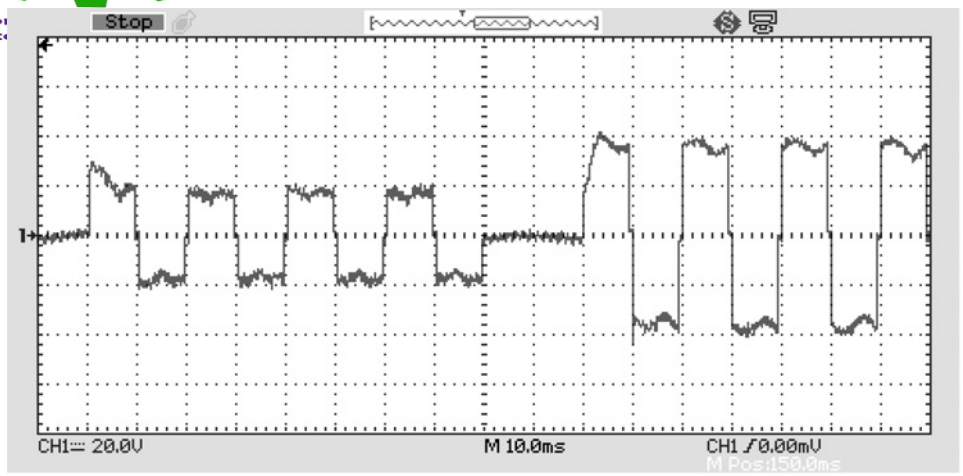
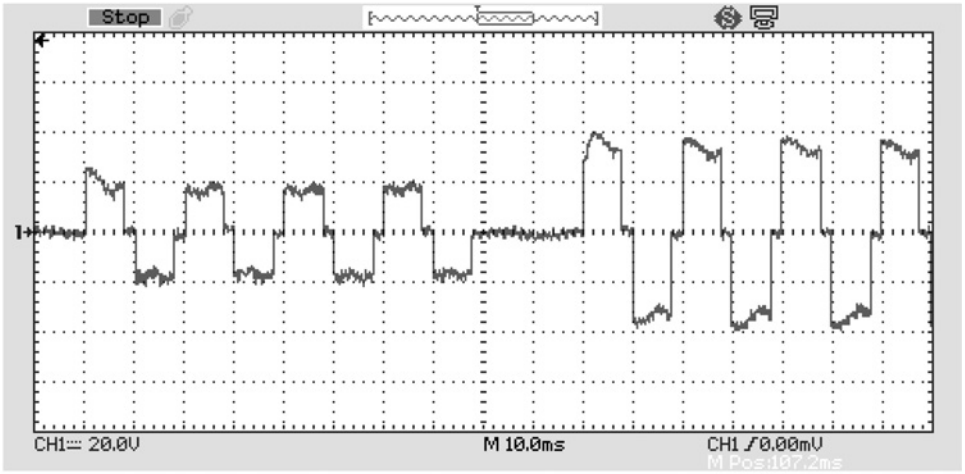


a



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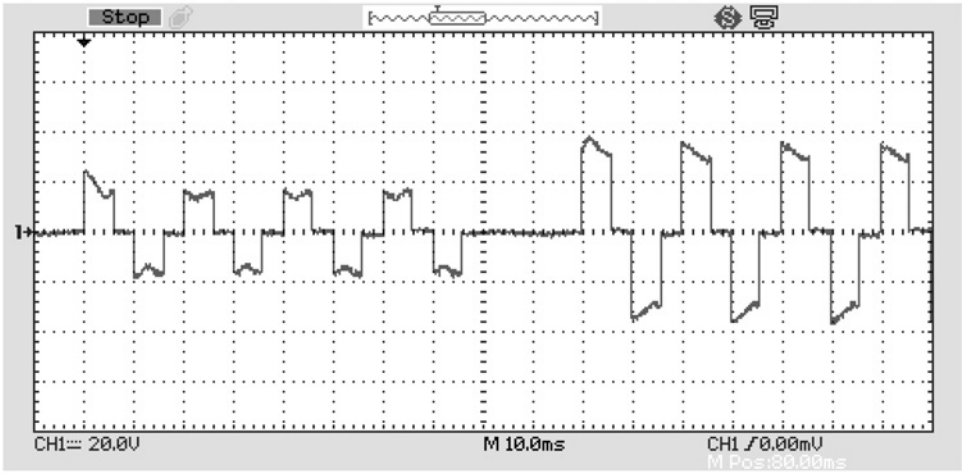

c

Fig. 12 *Experimental results*
a $v_{D,1}$
b $v_{D,2}$
c $v_{D,3}$
d $v_{D,4}$
e DC-link voltage

multilevel inverter. According to the figure, the THD of both the DVR output voltage and the load voltage in the proposed DVR is considerably lower than that of the conventional CHB multilevel inverter-based DVR. This is due to the fact that in the proposed DVR the dc-link voltage is regulated considering the voltage sag depth. As a result, the number of levels of the DVR output voltage remain constant regardless of voltage sag depth. Consequently, the THD value of the DVR output voltage in the proposed approach is much lower and also it can be considered constant. If a

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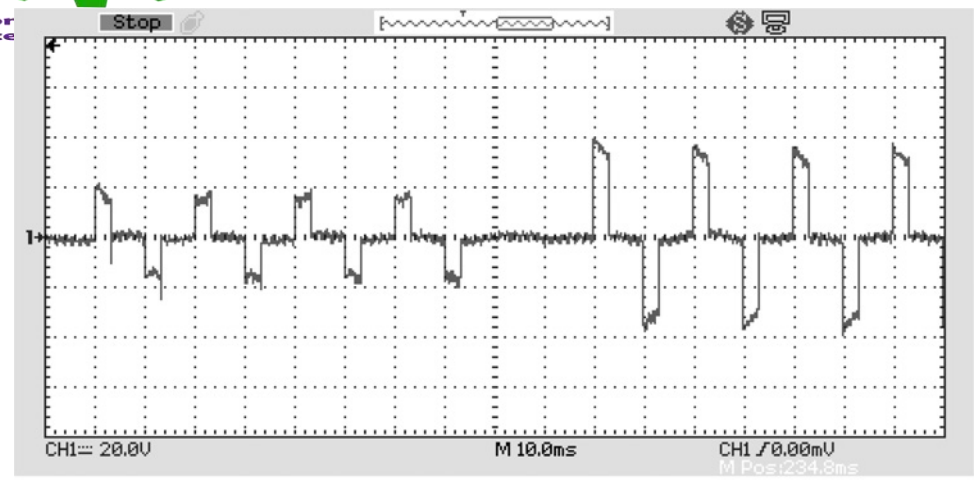

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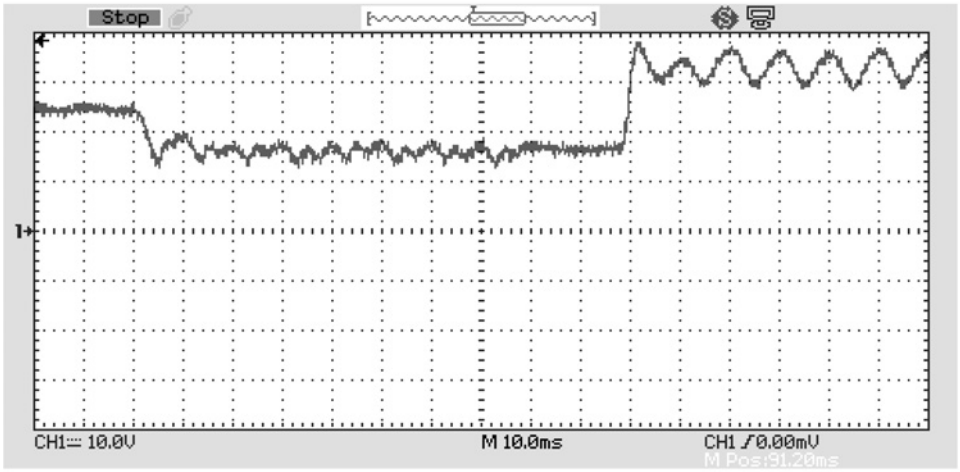

e

Fig. 12 *Continued*

THD of 5% is considered as a threshold for the load voltage, Fig. 9 suggests that the conventional approaches cannot use the aforementioned fundamental frequency method which has advantages such as lower number of commutations, lower switching losses and lower stress and EMI. Therefore the conventional approaches have to use HF modulation methods with an output filter.

4.2 Experimental results

The experimental results of the nine-level inverter-based laboratory prototype have been presented to demonstrate the proposed scheme in practice. The IGBTs used in the prototype are BUP306D with internal anti-parallel diodes with voltage and current ratings equal to 1200 V and 20 A, respectively. The 89C52 microcontroller by ATMEL Company is used to drive the switches. The input dc voltage of the boost dc–dc converter is provided by a dc voltage source existing in the laboratory. The experimental setup is based on an offline programmed microcontroller. In this method, different voltage sag scenarios are considered and the required switching actions of all the switches (switches of the DVR and the dc–dc converter) are stored in the microcontroller as look-up tables. Based on the value of the voltage sag, the microcontroller reads the corresponding look-up table and generates the switching signals. The look-up tables are essentially obtained from the simulation. In other words, the switching state of each switch during voltage sag is predetermined and stored in the microcontroller. This method provides a cheap and simple solution for the experimental setup. This approach can be represented by the flowchart shown in Fig. 10.

Using (5) and considering that $n = 4$, the values of the switching angles (see Fig. 6) can be obtained as follows

$$a_1 = 7.18^\circ, \quad a_2 = 22^\circ, \quad a_3 = 38.68^\circ, \quad a_4 = 61^\circ$$

The multilevel inverter switching table is based on the switching angles obtained above. Table 4 shows the switching table of the nine-level inverter in the proposed DVR. The first column shows the switching intervals and the corresponding output voltage levels are shown in the second column. The third column shows the switches that are turned on in each switching interval.

The measured experimental waveforms are shown in Fig. 11. The grid voltage is shown in Fig. 11*a*. Considering this figure, two different voltage sags are visible. Voltage sag with a depth of 0.2 pu and duration of four fundamental cycles occurs as the first case. Then, the grid voltage returns to its normal condition for a cycle. After that, the second voltage sag with a depth of 0.4 pu occurs. The DVR output voltage and the load voltage are shown in Figs. 10*c* and 11*b*, respectively. As these figures indicate, the DVR generates and injects the required compensation voltage in

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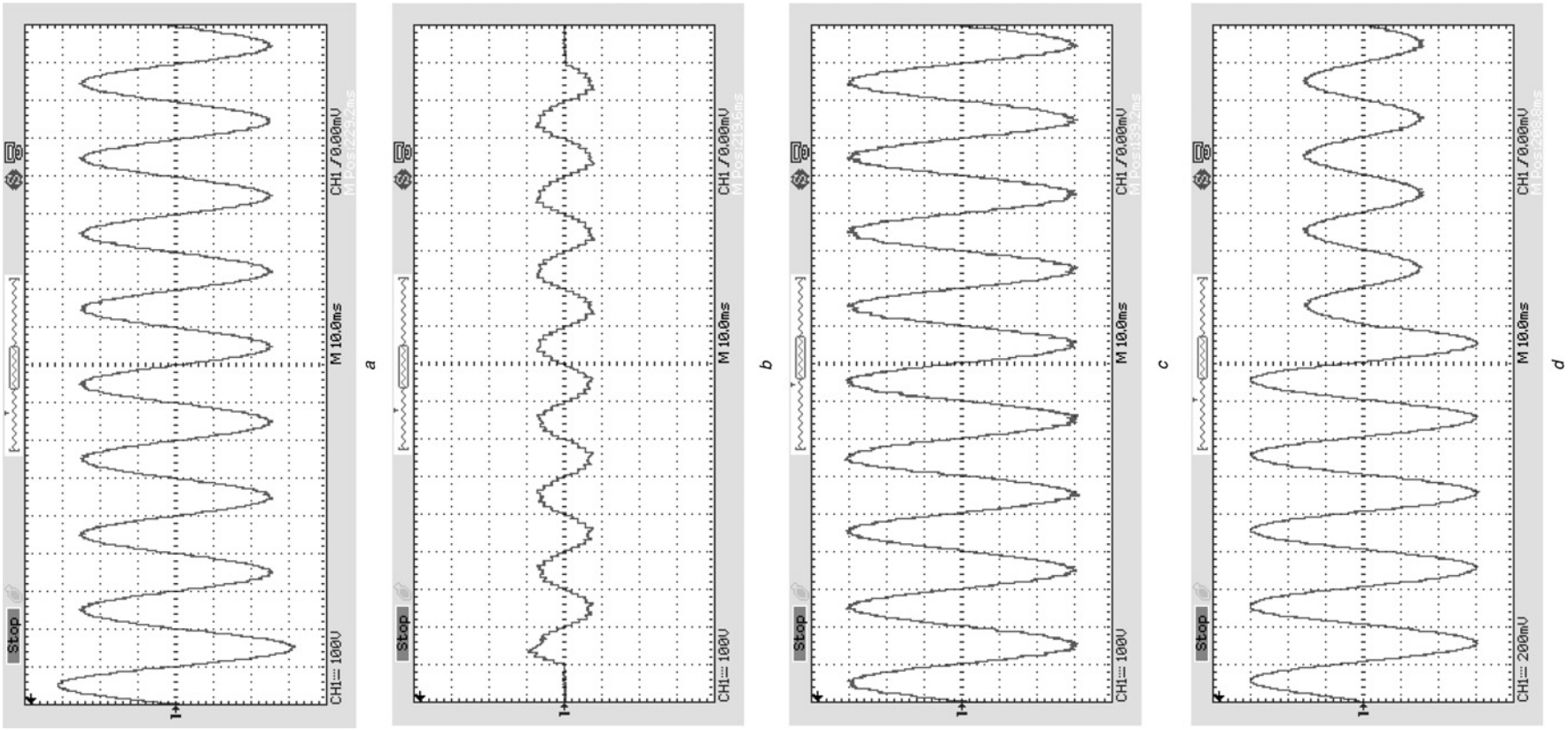

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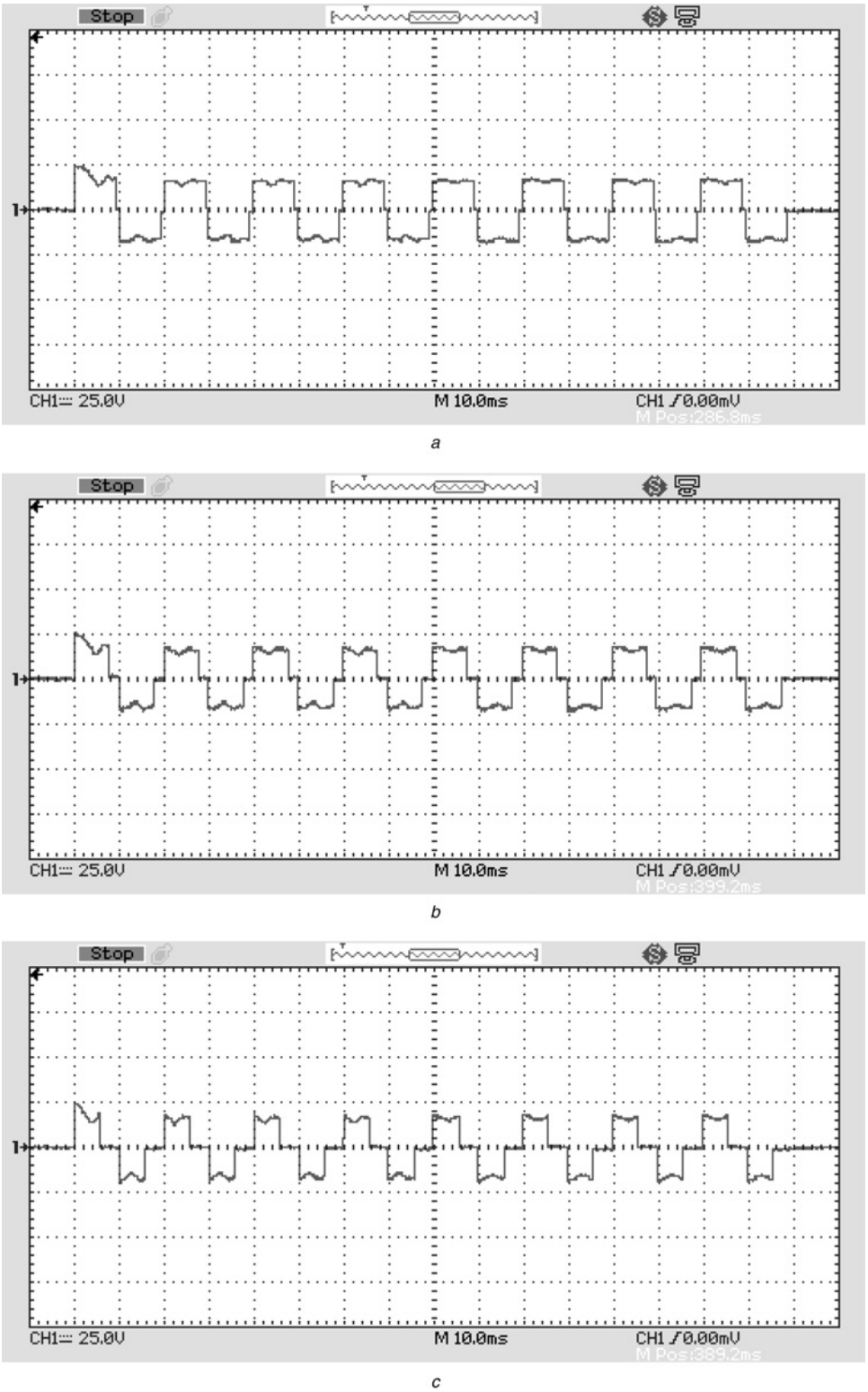

Fig. 14 *Experimental results for the case of abrupt variation of load*
a $v_{D,1}$
b $v_{D,2}$
c $v_{D,3}$
d $v_{D,4}$
e DC-link voltage

both voltage sag conditions and the load voltage is fully compensated for. It is important to note that nevertheless the voltage sag depth is different in the two voltage sag conditions; the output voltage of the DVR is a nine-level voltage in both conditions. This results in improved output

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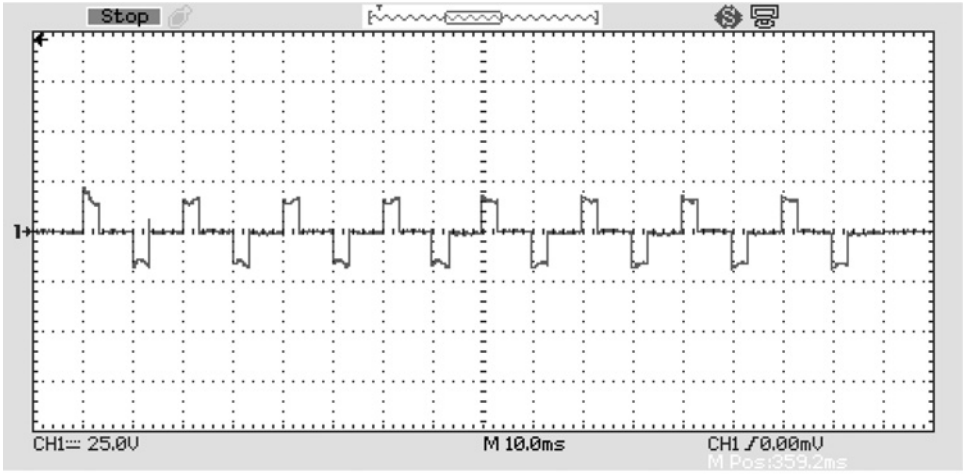
voltage quality and eliminating the filtering requirements which are the advantages of the proposed topology in comparison with the conventional multilevel inverter-based DVRs. Figs. 12*a–d* show the output voltage of the first, second, third and fourth bridge of multilevel inverter,



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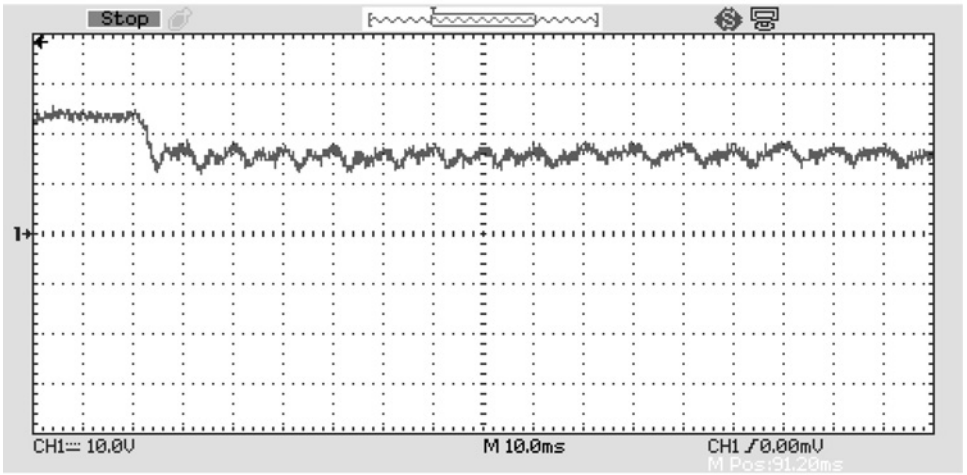

e

Fig. 14 *Continued*

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respectively. These experimental results verify the simulation results of Fig. 7*b*. The dc-link voltage (output voltage of the dc–dc converter) is shown in Fig. 12). As the figure shows, the dc–dc converter adjusts the dc-link voltage based on the value of voltage sag so that the maximum number of output voltage levels can be obtained in both voltage sag conditions.

Considering the experimental results and comparing them with the simulation results, a good correspondence is observed between the simulation and the experimental results.

Fig. 13 shows the experimental results for abrupt variations of the load. In this case, a 0.2 pu voltage sag is applied on the grid voltage. After four cycles of beginning of the voltage sag, abrupt variation of the load occurs. At this instant, the value of load resistance changes from 50 to 100 Ω and the value of the load inductance changes from 55 to 110 mH. In other words, the load impedance is doubled. Figs. 13*a–c* show the grid voltage, injected voltage and load voltage, respectively. As the figure shows, the DVR keeps compensating for the load voltage after abrupt change of the load. The load current is shown in Fig. 13*d* in order to verify abrupt variation of the load impedance. The output voltages of the bridges of the multilevel inverter are shown in Figs. 14*a–d*. Fig. 14*e* shows the output voltage of the dc–dc converter (dc-link voltage). Despite an abrupt change in the load, the dc–dc converter adjusts the dc-link voltage so that the desired compensation is achieved.

5 Conclusion

This paper proposed the multilevel inverter-based DVR with adjustable dc-link voltage. In the proposed scheme, a dc–dc converter is used to adjust the dc-link voltage of the multilevel inverter considering the voltage sag depth. As the mathematical analysis showed, in a wide range of voltage sag variations, the proposed DVR makes it possible to generate maximum possible number of voltage levels. The results of such a scheme are considerably improved quality of the output voltage, reduced or eliminated filtering requirements and possibility to work with a fundamental frequency control method (reduced switching losses). The simulation and experimental results of a nine-level inverter-based DVR, which were designed to compensate for up to 0.5 pu voltage sags, demonstrated the proposed scheme. For this case, for voltage sags between 0.16 and 0.5 pu, the output voltage is a nine-level voltage. This is not possible in the conventional approaches.

6 References

1 Babaei, E., Farhadi Kangarlu, M., Sabahi, M.: 'Mitigation of voltage disturbances using dynamic voltage restorer based on direct converters', *IEEE Trans. Power Deliv.*, 2010, 25, (4), pp. 2676–2683

2 Jiang, Y., Liu, H., Zheng, Q., Zheng, L.: 'A novel apparatus for adjusting the insertion voltage of transmission line based on variable inductors', *IEEE Trans. Power Deliv.*, 2012, 27, (1), pp. 23–31

International journal of imaging science and engineering

ISSN: 1934--9955 www.ijise.net

Vol-20 Issue-01 Mar 2025

3 Badrkhani Ajaei, F., Farhangi, S., Iravani, R.: 'Fault current interruption by the dynamic voltage restorer', *IEEE Trans. Power Deliv.*, 2013, 28, (2), pp. 903–910
4 Sasitharan, S., Mishra, M.K.: 'Constant switching frequency band controller for dynamic voltage restorer', *IET Power Electron.*, 2010, 3, (5), pp. 657–667
5 Babaei, E., Farhadi Kangarlu, M., Sabahi, M.: 'Compensation of voltage disturbances in distribution systems using single-phase dynamic voltage restorer', *Electr. Power Syst. Res.*, 2010, 80, (12), pp. 1413–1420
6 Visser, A.J., Enslin, J.H.R., Mouton, H.T.: 'Transformerless series sag compensation with a cascade multilevel inverter', *IEEE Trans. Ind. Electron.*, 2002, 49, (4), pp. 824–831
7 Loh, P.C., Vilathgamuwa, D.M., Tang, S.K., Long, H.L.: 'Multilevel dynamic voltage restorer', *IEEE Power Electron. Lett.*, 2004, 2, (4), pp. 125–130
8 Wang, B., Venkataramanan, G., Illindala, M.: 'Operation and control of a dynamic voltage restorer using transformer coupled H-bridge converters', *IEEE Trans. Power Electron.*, 2006, 21, (4), pp. 1053–1061
9 Al-Hadidi, H.K., Gole, A.M., Jacobson, D.A.: 'Minimum power operation of cascade inverter-based dynamic voltage restorer', *IEEE Trans. Power Del.*, 2008, 23, (2), pp. 889–898
10 Al-Hadidi, H.K., Gole, A.M., Jacobson, D.A.: 'A novel configuration for a cascade inverter-based dynamic voltage restorer with reduced energy storage requirements', *IEEE Trans. Power Deliv.*, 2008, 23, (2), pp. 881–888
11 Massoud, A.M., Ahmed, S., Enjeti, P.N., Williams, B.W.: 'Evaluation of a multilevel cascaded-type dynamic voltage restorer employing discontinuous space vector modulation', *IEEE Trans. Ind. Electron.*, 2010, 57, (7), pp. 2398–2410
12 Meyer, C., Romaus, C., DeDoncker, R.W.: 'Five level neutral-point clamped inverter for a dynamic voltage restorer'. Proc. European Conf. on Power Electronics and Applications, 2005
13 Barros, J.D., Silva, J.F.: 'Multilevel optimal predictive dynamic voltage restorer', *IEEE Trans. Ind. Electron.*, 2010, 57, (8), pp. 2747–2760
14 Roncero-Sanchez, P., Acha, E.: 'Dynamic voltage restorer based on flying capacitor multilevel converters operated by repetitive control', *IEEE Trans. Power Del.*, 2009, 24, (2), pp. 951–960
15 Frahadi Kangarlu, M., Hosseini, S.H., Babaei, E., Khoshkbar Sadigh, A.: 'Transformerless DVR topology based on multilevel inverter with reduced number of switches'. Proc. PEDSTC, 2010, pp. 371–375
16 Babaei, E., Hosseini, S.H., Gharehpetian, G.B., Tarafdar Haque, M., Sabahi, M.: 'Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology', *Electric Power Syst. Res.*, 2007, 77, (8), pp. 1073–1085
17 Babaei, E., Farhadi Kangarlu, M.: 'Operation and control of dynamic voltage restorer using single-phase direct converter', *Energy Convers. Manag.*, 2011, 52, (8–9), pp. 2965–2972
18 Babaei, E., Farhadi Kangarlu, M.: 'Voltage quality improvement by dynamic voltage restorer based on direct three-phase converter with fictitious dc link', *IET Gener. Transm. Distrib.*, 2011, 5, (8), pp. 814–823
19 Rosas-Caro, J.C., Mancilla-David, F., Ramirez-Arredondo, J.M., Bakir, A.M.: 'Two-switch three-phase ac-link dynamic voltage restorer', *IET Power Electron*, 2012, 5, (9), pp. 1754–1763
20 Zhang, L., Loh, P.C., Gao, F.: 'An integrated nine-switch power conditioner for power quality enhancement and voltage sag mitigation', *IEEE Trans. Power Electron.*, 2012, 27, (3), pp. 1177–1190
21 Wessels, C., Gebhardt, F., Fuchs, F.W.: 'Fault ride-through of a DFIG wind turbine using a dynamic voltage restorer during symmetrical and asymmetrical grid faults', *IEEE Trans. Power Electron.*, 2011, 26, (3), pp. 807–815
22 Babaei, E., Farhadi Kangarlu, M.: 'A new scheme for multilevel inverter based dynamic voltage restorer'. Proc. ICEMS; 2011, China
23 Kouro, S., Bernal, R., Miranda, H., Silva, C., Rodriguez, J.: 'High-performance torque and flux control for multilevel inverter fed induction motors', *IEEE Trans. Power Electron.*, 2007, 22, (6), pp. 2116–2123
24 Perez, M., Rodriguez, J., Pontt, J., Kouro, S.: 'Power distribution in hybrid multicell converter with nearest level modulation'. Proc. ISIE, 2007, Spain, pp. 736–741
25 Lee, D.M.: 'A voltage sag supporter utilizing a PWM-switched autotransformer'. PhD. Thesis, 2004, Georgia Institute of Technology, Atlanta
26 Brumsickle, W.E., Schneider, R.S., Luckjiff, G.A., Divan, D.M., McGranaghan, M.F.: 'Dynamic sag correctors: cost-effective industrial power line conditioning', *IEEE Trans. Ind. Appl.*, 2001, 32, (1), pp. 212–217
27 Yildirim, D., Fuchs, E.F.: 'Measured transformer derating and comparison with harmonic loss factor (F_{HL}) approach', *IEEE Trans. Power Deliv.*, 2000, 15, (1), pp. 186–191
28 Rodriguez, J., Franquelo, L.G., Kouro, S., *et al*: 'Multilevel converters: An enabling technology for high power applications', *Proc. IEEE*, 2009, 97, (11), pp. 1786–1817
29 Farhadi Kangarlu, M., Babaei, E.: 'Cross-switched multilevel inverter: an innovative topology', *IET Power Electron.*, 2013, 6, (4), pp. 642–651